IN THE CLAIMS:

Please amend the following claims:

2. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

4

D

3. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by the respective substrate potentials.

4. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate

includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

D4 cont'd

5. (Amended) A semiconductor integrated circuit according to claim 1, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials.

8. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

D5

9. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate

includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials of the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by respective potentials of the well regions thereof.

D5 cont'd

10. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

11. (Twice Amended) A semiconductor integrated circuit according to claim 6, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied

D5 cont'd

in a reverse direction by respective potentials in the well regions thereof.

D6

13. (Amended) A semiconductor integrated circuit according to claim 12, wherein said first potential pair includes a first high potential and a first low potential, said second potential pair includes a second high potential higher than said first high potential and a second low potential lower than said first low potential, and said substrate potential is one of a high potential side substrate potential between said first and second high potentials and a low potential side substrate potential between said first and second low potentials.

D7

17. (Amended) A semiconductor integrated circuit according to claim 16, wherein

said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes a second high potential line having a potential higher than that of said first high potential line and a second low potential line having a potential lower than said first low potential line, and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of said second high potential line, and a low potential side substrate potential line having a potential between the potential of said first low potential line and the potential of said second low potential line.

D7 cont'd

19. (Amended) A semiconductor integrated circuit according to claim 16, wherein said first potential line pair includes a first high potential line and a first low potential line,

said second potential line pair includes said first low potential line and a second high potential line having a potential higher than that of the first high potential line, and

said substrate potential line is one of a high potential side substrate potential line having a potential between the potential of said first high potential line and the potential of the second high potential line, and a low potential side substrate potential line having a potential higher than the potential of said first low potential line.

D8

21. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a substrate potential, and

said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

22. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials, and

said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by the respective substrate potentials.

23. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor to which substrate

bias is applied in a reverse direction by a substrate potential, and

said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by said substrate potential.

D9 cont'd

24. (Amended) A semiconductor integrated circuit according to claim 20, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective substrate potentials.

D10

37. (Twice Amended) A design data recording medium on which design data for forming an integrated circuit on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a well region on which a plurality of logic gates is formed;

second mask pattern data for determining a figure pattern for forming a first line pair, a second line pair and a third line pair on said well r gion; and

third mask pattern data for determining a figure pattern for forming a plurality of connectors,

wherein a first group of said connectors connects said first line pair and portions of said well region,

wherein a second group of said connectors connects said second line pair and a first group of said logic gates for supplying a first potential difference to said first group of logic gates in an active operation mode, and

wherein a third group of said connectors connects said third line pair and a second group of said logic gates for supplying a second potential difference which is larger than said first potential difference to said second group of logic gates in said active operation mode.

D10 cont'd

39. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by a potential in the well region thereof, and said second logic gate includes an MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

D11

40. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials of the well regions thereof, and said second logic gate includes a p-channel type MIS transistor and an n-channel type MIS transistor to which substrate biases are applied in a forward direction by respective potentials of the well regions thereof.

D11 cont'd

41. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a reverse direction by a potential of the well region thereof, and said second logic gate includes a p-channel type MIS transistor to which a substrate bias is applied in a forward direction by a potential in the well region thereof.

42. (Amended) A semiconductor integrated circuit according to claim 7, wherein said first logic gate includes a p-channel type MIS transistor and an n-channel

type MIS transistor to which substrate biases are applied in a reverse direction by respective potentials in the well regions thereof.

Please add the following claims:

43. (New) A semiconductor integrated circuit according to claim 1, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

44. (New) A semiconductor integrated circuit according to claim 6, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

45. (New) A semiconductor integrated circuit according to claim 7, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

46. (New) A semiconductor integrated circuit according to claim 12, wherein said first and second logic

gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

47. (New) A semiconductor integrated circuit according to claim 16, wherein said first and second logic gates are connected to said first and second potential line pairs, respectively, in a standby mode.

48. (New) A semiconductor integrated circuit according to claim 20, wherein said first and second logic gates are supplied with said first and second potential pairs, respectively, as power sources in a standby mode.

D12 cont'd

49. (New) A semiconductor integrated circuit according to claim 37, wherein said first and second groups of logic gates are supplied from said second and third line pairs, respectively, in a standby mode.

50. (New) A semiconductor integrated circuit according to claim 38, wherein said first and second logic gates are supplied from said first and second potential line pairs, respectively, in a standby mode.

51. (New) A semiconductor integrated circuit comprising:

a first logic gat which is supplied with a first potential difference as a sole operation power source from a first line pair; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second line pair,

wherein said first potential difference is smaller than said second potential difference, and

wherein a substrate potential of MIS transistors is commonly used by said first and second logic gates.

D12 cont'd

52. (New) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first line pair; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second line pair,

wherein said first potential difference is smaller than said second potential difference, and

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor

of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are made common for each conduction type.

53. (New) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from a first line pair; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second line pair,

wherein said first potential difference is smaller than said second potential difference, and

wherein said first and second logic gates have MIS transistors, and a well region in which an MIS transistor of said first logic gate is formed and a well region in which an MIS transistor of said second logic gate is formed are electrically connected for each conduction type.

54. (New) A semiconductor integrated circuit comprising:

a first logic gate which is supplied with a first potential difference as a sole operation power source from

a first line pair of a high potential and a low potential; and

a second logic gate which is supplied with a second potential difference as a sole operation power source from a second line pair of a high potential and a low potential,

wherein said first potential difference is smaller than said second potential difference,

wherein a substrate potential of an MIS transistor in said first logic gate and that of an MIS transistor in said second logic gate are common to each other, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

D12 cont'd

55. (New) A semiconductor integrated circuit comprising:

a first logic gate connected to receive a first potential difference as a sole operation power source from a first pair of a high potential line and a low potential line; and

a second logic gate connected to receive a second potential difference as a sole operation power source from a second pair of a high potential line and a low potential

line,

wherein said first potential difference is smaller than said second potential difference,

wherein a substrate potential line is commonly used for supplying a substrate potential to an MIS transistor of said first logic gate and for supplying a substrate potential to an MIS transistor of said second logic gate, and

at least said first logic gate includes an MIS transistor to which a substrate bias is applied in a reverse direction by said substrate potential.

D12 cont'd

56. (New) A semiconductor integrated circuit having a circuit region in which a number of logic gates each having an MIS transistor are arranged on a semiconductor substrate,

wherein said circuit region has a well region including portions shared by a substrate potential for each conduction type of MIS transistor,

a first logic gate is supplied with a first potential difference as a sole operation power source from a first line pair,

a second logic gate is supplied with a second

potential difference as a sole operation power source from a second line pair,

said first logic gate and said second logic gate are formed in said well region,

said first potential difference is smaller than said second,

in said well region, a p-type well portion in which an n-channel type MIS transistor is formed and an n-type well portion in which a p-channel type MIS transistor is formed are adjacent to each other, and

metal lines for supplying said first potential difference, said second potential difference, and a substrate potential are arranged on said well region.

D12 cont'd

57. (New) A design data recording medium on which design data for forming an integrated circuit on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first mask pattern data for determining a figure pattern for forming a well region on which a plurality of logic gates is formed,

second mask pattern data for determining a figure pattern for forming a first line pair, a second line pair and a third line pair on said well region, and

third mask pattern data for determining a figure pattern for forming a plurality of connectors,

wherein a first group of said connectors connects said first line pair and portions of said well region,

wherein a second group of said connectors connects said second line pair and a first group of said logic gates for supplying said first group of logic gates with a first potential difference as a sole operation power source from said second line pair, and

wherein a third group of said connectors connects said third line pair and a second group of said logic gates for supplying said second group of logic gates with a second potential difference, which is larger than said first potential difference, as a sole operation power source from said third line pair.

D2 cont'd

58. (New) A design data recording medium on which design data for designing an integrated circuit to be formed on a semiconductor chip is recorded so as to be readable by a computer, the design data comprising:

first function description data for determining a function of a first logic gate which is supplied with a first potential difference as a sole operation power source from a first pair of potential lines and a substrate potential from a substrate potential line;

second function description data for determining a function of a second logic gate which is supplied with a second potential difference as a sole operation power source from a second pair of potential lines and a substrate potential from said substrate potential line; and

third function description data for determining said first potential difference to be smaller than said second potential difference.

59. (New) A design data recording medium according to claim 58,

wherein said well region includes a first well portion and a second well portion,

wherein said first mask pattern data includes fourth mask pattern data and fifth mask pattern data,

wherein said fourth mask pattern data is for determining a figure pattern for forming the first well portion, and

D12 cont'd

wherein said fifth mask pattern data is for determining a figure pattern for forming the second well portion.